METHOD FOR USING A PRE-CONFIGURED TDM SWITCH AND TRAFFIC DISCARD TO FACILITATE UPSR SELECTION

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is filed concurrently with a commonly-owned application entitled METHOD FOR USING A PRE-CONFIGURED ATM SWITCH AND TRAFFIC DISCARD TO FACILITATE UPSR SELECTION.

TECHNICAL FIELD OF THE INVENTION

This invention relates to technology in a digital network and more particularly to techniques for protection switching of SONET UPSR.

BACKGROUND OF THE INVENTION

The synchronous optical network (SONET) standards for optical transmission include a number of mechanisms and recommendations for protecting transmitted traffic. These include making use of "rings" that contain all of the transmission termination points. Such rings provide two paths between each transmission point on the ring, thus providing a level of redundancy. There are two basic ways to exploit SONET rings to protect traffic: a uni-directional path switched ring (UPSR) and a bi-directional line switched ring (BLSR).

A UPSR operates by having two copies of the same traffic go in opposite directions from one side of a SONET ring to the other. At the exit point from the ring, the traffic from the two directions is compared, and the better version is selected for output. This approach can be utilized for time division multiplexed (TDM) traffic using virtual tributary (VT) comparison. Specifically, the overhead associated with each VT that provides performance indications is inspected to determine which path exhibits better performance by whatever performance criteria is chosen.

Traditional approaches to UPSR for TDM involve switch reconfiguration. Specifically, a TDM switch is provided at the ring node where the VT is being extracted from the ring. The TDM switch is configured to switch the TDM traffic from one of the two VT copies through to a destination. When the VT performance measures indicate that the VT copy being discarded has become the superior or preferred version of the two VT copies, the TDM switch is reconfigured to switch through this VT copy and to

ignore the original VT copy. Such reconfigurations can be carried out indefinitely.

This type of TDM switch reconfiguration approach severely taxes the processing resources, such as a microprocessor (or other computing entity) that is controlling the switch. Reconfiguration is often a computationally involved task. The SONET standards require that switch reconfiguration occur within 50 ms of the failure of a transmission link that is carrying the active VT copy. This standard may not always be met under certain conditions.

SUMMARY OF THE INVENTION

According to the invention, SONET UPSR protection is effected by configuring a TDM switch to route TDM traffic from two receive circuits to the same destination. Based on UPSR traffic qualification, one copy of this traffic is discarded in the TDM switch so that only a single copy is passed to the TDM switch. Based upon received performance measurements, the circuit performing the discard operation can change. The same or similar mechanism can be used to protect against equipment failure and accommodate removal of one of the receive circuits.

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In a particular embodiment, an apparatus includes a number of receive circuits coupled to monitor signals on respective paths to a TDM switch. Each receive circuit sets a kill-bit to accompany TDM traffic sent to the TDM switch to indicate whether the TDM traffic should be switched or discarded. A memory coupled to the receive circuits receives the TDM traffic with accompanying kill-bits and stores the TDM traffic having an accompanying kill-bit that has not been set. The memory discards the TDM traffic having an accompanying kill-bit that has been set. A communication path between the receive circuits conveys qualifying information for the paths.

This overall approach, including configuration of the TDM switch such that it routes both VT copies through to the destination, allows for very fast switch-overs between VT copies. These switch-overs are achieved using decentralized processing in the receive circuits, with controlling messages sent between those circuits. Therefore, the processing drain for any microprocessor

controlling the TDM switch due to switch-overs may be reduced or eliminated. Other technical advantages are readily apparent to one skilled in the art from the following description, figures, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and for further features and advantages, reference is now made to the following description taken in conjunction with the accompanying drawings, where like reference numerals represent like parts, in which:

FIGURE 1 is a block diagram of a TDM communication network according to the invention; and

FIGURE 2 is a block diagram of components in a node of the network illustrating the function of a TDM switch in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

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FIGURE 1 is a block diagram of a TDM communication network 10 according to the invention. The nodes 12, 14, 16 and 18 may each include TDM switches as described below. Signal source 13 routes its traffic into node 12 which directs duplicate signals to node 18 via two paths, one though node 14 and node 16 and the other to node 18. Node 18 receives both signals, selects the best or preferred signal, and routes the selected signal to a destination 19.

Referring to FIGURE 2, at node 18, a TDM switch 22 can switch both VT copies through to destination 19. Kill-bits inserted by receive circuits 24, 26 control which VT copy is actually switched through on a byte-by-byte basis. In a particular embodiment, VT copies sent from receive circuits 24, 26 include the original eight bits and an additional kill-bit (nine bits total).

Receive circuits 24, 26 couple to a memory 20 for storing and forwarding traffic to TDM switch 22. Memory 20 stores an eight bit value for communication to TDM switch 22 if the kill-bit (9th bit) is not set. If the kill-bit is set, memory 20 discards or does not write the corresponding eight bit value to memory. Receive circuits 24, 26 exchange messages using bus 34 and/or link 38 to determine, based on VT performance measurements, the better VT copy. Based on this determination, one of the two receive circuits 24, 26 sets kill-bits to prevent writing of VT copies to memory 20. The other receive circuit 24, 26 does not set kill-bits so that its VT copies are written to memory 20 and passed to TDM switch 22. The receive circuit 24, 26 that

sets kill-bits to indicate discard can change based on changes in VT performance measurements.

For the purposes of selecting between two copies, VTs and STS-1 paths are qualified using the following criteria:

1. Alarm indication signal (AIS), loss of pointer (LOP), or terminating circuit card missing;

2. Bit error rate (BER) exceeding 10^{-3} in the path, or other selected value; and

3. Signal degradation (SD) resulting from a BER exceeding 10^{-5} to 10^{-9}, or other selected value.

To perform the VT qualification, each receive circuit 24, 26 includes a decision module 30, 32 having memory and processing capabilities to perform the VT qualification. Decision modules 30, 32 each communicate information using bus 34 supported by control module 36. In a particular embodiment, bus 34 is functionally a cross-connect DS-0 implemented using a time-slot interchanger in control module 36. Decision modules 30, 32 may also communicate information for VT qualification using link 38 between receive circuits 24, 26. In one embodiment, link 38 supports a periodic keep-alive signal between receive circuits 24, 26 to detect equipment failure and/or removal, whereas bus 34 supports communication of qualification criteria between circuits 24, 26, such as AIS, LOP, BER, and SD.

In a particular embodiment, communications between receive circuits 24, 26 occur in a master/slave environment. For purposes of this discussion assume receive circuit 24 is the master circuit, while receive circuit 26 is the slave circuit. In this embodiment,

receive circuit 26 reports the qualification status of each VT upon which it receives traffic. Receive circuit 24 also determines the qualification status of each VT upon which it receives traffic, and also receives reports from receive circuit 26. Receive circuit 24 then selects, based on the qualification criteria, the active receive circuit 24, 26 to pass the VT traffic to TDM switch 22. The designation of master and slave may not change, but the active and stand-by status of receive circuits 24, 26 for passing particular VT traffic may change.

In operation, each receive circuit 24, 26 determines the VT for each received telephony byte, block, packet, or other portion of information, and performs a look-up in a table maintained by decision modules 30, 32. For each VT, the table includes a pass-through bit or other indicator specifying whether the particular VT carries pass-through traffic not intended for destination 19. For example, pass-through traffic may include information passed through node 18 from node 16 to node 12 or information passed through node 18 from node 12 to node 16. If the pass-through bit indicates pass-through traffic, then no further VT qualification processing is performed. In a particular embodiment, control module 36 populates tables maintained by decision modules 30, 32 with pass-through bits for each provisioned VT. If the pass-through bit for the determined VT indicates that information is to be routed to destination 19, then a qualification bit or other indicator specifies which receive circuit 24, 26 is currently active (passing

traffic to TDM switch 22) and which receive circuit 24, 26 is stand-by (discarding traffic).

In the particular embodiment illustrated in FIGURE 2, receive circuit 24 receives a telephony byte from node 16 on a particular VT, and decision module 30 performs a table look-up using the VT to determine that this byte is not pass-through (e.g., pass-through bit is set to zero), and that receive circuit 24 is active (e.g., qualification bit is set to one). As a result, receive circuit 24 does not set the kill-bit so that memory 20 stores the byte for communication to TDM switch 22. Receive circuit 26 receives a copy of the byte from node 12, performs a table look-up at decision module 32 using the same VT, and determines that this is not pass-through traffic, but that receive circuit 26 is stand-by for this particular VT. As a result, receive circuit 26 sets the kill-bit so that memory 20 does not store the byte.

For a variety of reasons, receive circuit 24 as the master may determine that it should no longer be active. This determination may be made based on the receipt at receive circuits 24, 26 of management traffic passed through or injected in the communication path from signal source 13 to node 18. For example, node 14 may detect an AIS condition between node 12 and node 14 due to, for example, an optical fiber cut. In this situation, node 14 inserts management traffic for transmission to node 18 through node 16. Receive circuit 24 receives the management traffic and determines that receive circuit 26 should be active. Receive circuit 24, still acting as master, sets the qualification bit in the table

maintained by decision module 30 to indicate that receive circuit 24 is stand-by, and sends a message using bus 34 or link 38 to command receive circuit 26 to operate as active. Receive circuit 26 sets the qualification bit in the table maintained by decision module 32 to indicate that receive circuit 26 is active, and begins passing bytes to be stored by memory 20 for communication to TDM switch 22.

A similar operation can take place if receive circuit 24 receives management or overhead traffic containing BER, SD, or other qualification criteria for the particular VT. This overhead or management traffic may either be sent as bad messages to indicate a degrade or loss in signal, or as periodic polling messages that, if absent, may indicate a degrade or loss in signal. Moreover, receive circuit 26 may perform a switch-over to active upon the detection of a loss of a keep-alive signal from receive circuit 24 over link 38. Therefore, receive circuits 24, 26 contemplate both VT level and card or circuit level metrics for qualification of signals. In any of these various embodiments, receive circuits 24, 26 communicate over bus 34 and/or link 38 to allow decision modules 30, 32 to determine the active/stand-by status of receive circuits 24, 26.

If SONET UPSR is being applied to STS-1 type blocks (possibly forming larger STS-N signals), the same general approach can be applied. That is, TDM switch 22 can be configured to switch through both copies of an STS-1 block arriving in two directions around a UPSR ring. STS-1 path level performance indications are used by

receive circuits 24, 26 to determine in a distributed manner which should set kill-bits to force the discard of its copy of the STS-1.

This UPSR approach, whether used for TDM or STS-1 traffic, can be generalized to select between two copies of any traffic stream coming from any two directions, regardless of whether or not the two traffic streams actually pass over SONET rings or other network configurations. This approach can be further generalized to select between traffic from a number of sources (more than two), including from redundant switches within the same unit.

Although the present invention has been described with several embodiments, a myriad of changes, variations, alterations, transformations, and modifications may be suggested to one skilled in the art, and it is intended that the present invention encompass such changes, variations, alterations, transformations, and modifications as fall within the scope of the appended claims.